UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/924,934	08/08/2001	Matthew C. Mattina	1662-38300 JMH (P01-3570)	3940

22879	7590	02/06/2006	EXAMINER	
			ANYA, CHARLES E	

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ART UNIT	PAPER NUMBER
2194	

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
	09/924,934	MATTINA ET AL.
Office Action Summary	Examiner	Art Unit	
	Charles E. Anya	2194	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3/ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *14 November 2005*.

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-34* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-34* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

WILLIAM THOMSON
SUPERVISORY PATENT EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1.   Claims 1-34 are pending in this application.

Claim Rejections - 35 USC § 112

2.   The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3.   Claim 3 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 3 as claimed indicates that **an owner processor is capable of executing multiple threads concurrently**, however the Examiner could not find in the specification where this claim limitation is either implicitly or explicitly disclosed.

Please indicate in the next response where in the specification this limitation is disclosed.

Claim Rejections - 35 USC § 102

4.   The following is a quotation of the appropriate paragraphs of 35

U.S.C. 102 that form the basis for the rejections under this section made in this

Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5.   **Claims 1,2,13,14,16,24 and 25 are rejected under 35 U.S.C. 102(b) as**

being anticipated by U.S. Pat. No. 5,887,138 to Hagersten et al.

6.   As to claim 1, Hagersten teaches a distributed multiprocessing computer

system, which includes a plurality of processors each coupled to an associated

memory module, wherein each associated memory module may store data that

is shared between said processors (figures 1-2), said system comprising: a

Home processor that includes a memory block and a directory for said memory

block in an associated memory module (Home Node/SMP 12 (Directory

66/Memory 22) Col. 7 Ln. 6 – 61, figure 2 Col. 10 Ln. 59 – 67, Col. 14 Ln. 13 –

24); an Owner processor that includes a cache memory (Requesting

Node/SMP12 (External Caches 18) Col. 7 Ln. 6 – 47, Col. 8 Ln. 10 – 29), and

wherein said Owner processor obtains an exclusive copy of said memory block,

and stores said exclusive copy of said memory block in said cache memory

("...cache data..." Col. 9 Ln. 18 – 25, Col. 9 Ln. 54 – 57, "When clear..." Col. 15

Ln. 33 – 39, Col. 19 Ln. 10 – 34); and wherein said Owner processor may

displace the exclusive copy of said memory block, and return said displaced copy

of said memory block to said Home processor with a signal indicating that said

Owner processor remains a sharer of said memory block ("…discarded…shared

state…" Col. 13 Ln. 21 – 39).

7.   As to claim 2, Hagersten teaches the distributed multiprocessing computer

system of claim 1, wherein said Owner processor obtains an exclusive copy of

said memory block by issuing a Load Lock instruction, and wherein the directory

associated with the Home processor indicates that said Owner processor has

obtained exclusive control of said memory block (Directory 66 Col. 19 Ln. 15 –

34).

8.   As to claims 13 and 24, see the rejection of claim 1 above.

9.   As to claims 14 and 25, see the rejection of claim 2 above.

10.   As to claim 16, Hagersten teaches the method of claim 13, wherein the act

of updating the coherence directory includes modifying a register to indicate that

the Owner processor has an exclusive copy of the memory block ("…updates…"

Col. 19 Ln. 28 – 30).

11.   **Claims 3 and 26 are rejected under 35 U.S.C. 103(a) as being**

unpatentable over U.S. Pat. No. 5,887,138 to Hagersten et al. in view of U.S.

Pat. No. 6,438,671 B1 to Doing et al.

12.	As to claim 3, Hagersten teaches the distributed multiprocessing computer system of claim 2, wherein said Owner processor is capable of displacing data associated with a non-executing thread from its associated cache memory ("...discarded..." Col. 13 Ln. 21 – 39).

13.	Hagersten is silent with reference to an Owner processor is capable of executing multiple threads concurrently.

14.	Hagersten teaches an Owner processor is capable of executing multiple threads concurrently (Col. 3 Ln. 45 – 64, Col. 4 Ln. 15 – 17).

15.	It would have been obvious to one of ordinary skill in the art at the time invention was to combine the teachings of Doing and Hagersten because the teaching of Doing would improve the system of Hagersten by providing a means that removes the need for a processor to wait for certain short term latency events, such as re-filling an instruction pipeline (Col. 3 Ln. 57 – 60).

16.	As to claim 26, see the rejection of claim 3 above.

**17.	Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,887,138 to Hagersten et al. in view of U.S. Pat. 6,425,050 B1 to Beardsley et al.**

18.   As to claim 15, Hagersten does not explicitly teach the method of claim

13, wherein the Load Lock instruction forms part of a Load Lock/store Conditional

instruction pair.

19.   Beardsley teaches the method of claim 13, wherein the Load Lock

instruction forms part of a Load Lock/store Conditional instruction pair

("...stages...destages..." Col. 4 Ln. 38 – 67).

20.   It would have been obvious to one of ordinary skill in the art at the time the

invention was made to combine the teachings of Beardsley and Hagersten

because the teaching of Beardsley would improve the system of Hagersten by

preventing delay in responding to a read request when a track is being destaged

in mission critical systems (Beardsley Col. 2 Ln. 46 – 60).

21.   Claims 4,17 and 27 are rejected under 35 U.S.C. 103(a) as being

unpatentable over U.S. Pat. No. 5,887,138 to Hagersten et al. in view of U.S.

Pat. No. 6,438,671 B1 to Doing et al. as applied to claim 3 above, and further

in view of U.S. Pat. No. 5,937,199 to Temple.

22.   As to claim 4, Both Doing and Hagersten are silent with reference to the

distributed multiprocessing computer system of claim 3, wherein said Owner

processor includes a register in which an address is stored representing the

memory block obtained in response to the Load Lock instruction, and wherein

said Owner processor compares the address of any displaced data with the

address stored in said register.

23.   Temple teaches the Owner processor to include a register in which an

address is stored representing the memory block obtained in response to the

Load Lock instruction, and wherein said Owner processor compares the address

of any displaced data with the address stored in said register (Col. 10 Ln. 5 - 36).

24.   It would have been obvious to one of ordinary skill in the ad at the time the

invention was made to combine the teachings of Temple, Doing and Hagersten

because the teaching of Temple would improve the system of Doing and

Hagersten by providing a read-modify-write operation that ensures that a storage

location from which data is accessed is not subsequently accessed by the

system prior to the storage of the modified data (Temple Col. 10 Ln. 10 - 14).

25.   As to claims 17 and 27, see the rejection of claim 4 above.

26.   Claims 5-7,18,19,28 and 29 are rejected under 35 U.S.C. 103(a) as

being unpatentable over U.S. Pat. No. 5,887,138 to Hagersten et al. in view

of U.S. Pat. No. 6,438,671 B1 to Doing et al. as applied to claim 3 above, and

further in view of U.S. Pat. No. 5,937,199 to Temple, and further in view of

U.S. Pub. No. 2001/0010068 A1 to Michael et al.

27.   As to claim 5, Neither Temple, Doing nor Hagersten teaches the

distributed multiprocessing computer system of claim 4, wherein the Owner

processor asserts a Victim To Shared message if the address of any displaced

data matches the address stored in said register.

28.   Michael teaches the distributed multiprocessing computer system of claim 4, wherein the Owner processor asserts a Victim To Shared message if the address of any displaced data matches the address stored in said register.

29.   It would have been obvious to one of ordinary skill in the ad at the time the invention was made to combine the teachings of Michael, Temple, Doing and Hagersten because the teaching of Temple would improve the system of Temple, Doing and Hagersten by providing a cache system that minimizes directory cache pollution, leading to higher directory hit ratios and resulting improvement in system performance (Michael page 2 paragraph 0014).

30.   As to claim 6, Michael teaches the distributed multiprocessing computer system of claim 5, wherein the Owner processor assets a Victim message if the address of any displaced data does not match address stored in said register ("...not changed..." page 2 paragraph 0034).

31.   As to claim 7, Michael teaches the distributed multiprocessing computer system of claim 5, wherein the directory associated with the Home processor indicates that said Owner processor has become a sharer of said memory block in response to said Victim To Shared message ("...set..." page 2 paragraph 0034).

32.   As to claims 18 and 28, see the rejection of claim 5 above.

33.   As to claims 19 and 29, see the rejection of claim 7 above.

34.   Claims 8-12,20-23 and 30-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,887,138 to Hagersten et al. in view of U.S. Pat. No. 6,438,671 B1 to Doing et al. as applied to claim 3 above, and further in view of U.S. Pat. No. 5,937,199 to Temple, and further in view of U.S. Pub. No. 2001/0010068 A1 to Michael et al., and further in view of U.S. Pat. 6,425,050 B1 to Beardsley et al.

35.   As to claim 8, Neither Michael, Temple, Doing nor Hagersten teach the distributed multiprocessing computer system of claim 7, wherein said Owner processor subsequently re-obtains an exclusive copy of said memory block to complete execution of the non-executing thread.

36.   Beardsley teaches the distributed multiprocessing computer system of claim 7, wherein said Owner processor subsequently re-obtains an exclusive copy of said memory block to complete execution of the non-executing thread (Col. 7 Ln. 1 - 11).

37.   It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Beardsley, Michael, Temple, Doing and Hagersten because the teaching of Beardsley would improve the system of Michael, Temple, Doing and Hagersten by preventing delay in responding to a read request when a track is being destaged in mission critical systems (Beardsley Col. 2 Ln. 46 – 60).

38.   As to claim 9, Beardsley teaches the distributed multiprocessing computer

system of claim 8, wherein the Owner processor assets a Read-with-Modify

Intent Store Conditional instruction to the Home directory/processor to again

request an exclusive copy of said memory block (Col. 7 Ln. 1 - 11).

39.   As to claim 10, Beardsley teaches the distributed multiprocessing

computer system of claim 9, wherein, in response to the Read-with-Modify Intent

Store Conditional instruction, the Home directory/processor determines if the

Owner processor is a sharer of the memory block, and if so, the Home directory

sends an exclusive copy of the memory block to the Owner processor (Col. 7 Ln.

1 - 11).

40.   As to claim 11, Beardsley teaches the distributed multiprocessing

computer system of claim 10, wherein the Home directory/processor invalidates

all other sharers when it sends an exclusive copy of the memory block to the

Owner (Col. 7 Ln. 7 - 11).

41.   As to claim 12, Beardsley teaches the distributed multiprocessing

computer system of claim 9, wherein the Home directory determines if the Owner

processor is a sharer of the memory block, and if not, the Home

directory/processor sends a Store Conditional Failure message to the Owner

processor (Col. 7 Ln. 7 - 11).

42.   As to claims 20 and 31, see the rejection of claim 9 above.

43.   As to claims 21 and 32, see the rejection of claim 10 above.

44.   As to claims 22 and 33, see the rejection of claim 11 above.

45.   As to claims 23 and 34, see the rejection of claim 12 above.

46.   As to claim 30, see the rejection of claim 8 above.

Conclusion

Any inquiry concerning this communication or earlier communications from

the examiner should be directed to Charles E. Anya whose telephone number is

(571) 272-3757. The examiner can normally be reached on M-F (8:30-6:00) First

Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the

examiner's supervisor, An Meng-Ai can be reached on (571) 272-3756. The fax

phone number for the organization where this application or proceeding is

assigned is 703-872-9306.

Information regarding the status of an application may be obtained from

the Patent Application Information Retrieval (PAIR) system. Status information

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system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-

free).

Charles E Anya
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WILLIAM THOMSON
SUPERVISORY PATENT EXAMINER